

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Ryu OGIWARA et al.

Serial No.: Continuation of 10/372,886, filed
February 26, 2003

Filed: Herewith

For: FERROELECTRIC MEMORY AND
SEMICONDUCTOR MEMORY

Atty. Docket No.: 1701.00198

Group Art Unit: Unknown

Examiner: Unknown

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with Applicants' duty of disclosure, the following information is submitted for consideration by the United States Patent and Trademark Office in connection with the above-captioned application. The information is identified on the attached PTO-1449 form.

This application relies, under 35 U.S.C. § 120, on the earliest filing date of prior U.S. patent application serial nos. 10/372,886, filed February 26, 2003; 10/228,067, filed August 27, 2002; and 09/585,081, filed June 1, 2000. The documents identified on the attached PTO 1449 form were submitted to and/or cited by the Office in a prior application and, therefore, copies are not required to be provided in this application. (See 37 C.F.R. § 1.98(d)).

Applicants do not waive any right to take appropriate action to establish patentability over the listed documents should they be applied as references against the claims of the present application.

It is respectfully requested that the Examiner fully consider each of the documents, initial the enclosed Form PTO-1449 in the appropriate place to indicate that the document has been

considered, and return a copy of the initialed form to the undersigned in accordance with MPEP Section 609.

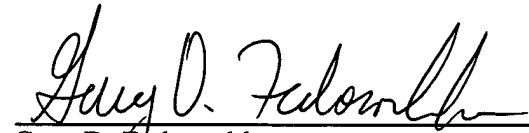
Applicants believe that no fee is necessary pursuant to 37 C.F.R. § 1.97(b). However, if a fee is due, the Office is authorized to charge Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: December 24, 2003

By:

A handwritten signature in dark ink, appearing to read "Gary D. Fedorochko", is written over a horizontal line.

Gary D. Fedorochko

Registration No. 35,509

1001 G Street, N.W.
Washington, D.C. 20001-4597
(202) 508-9100

GDF:lab

Please type a plus sign (+) inside this box → +

PTO/SB/08A (08-00)

Approved for use through 10/31/2002. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known

Application Number	TBA
Filing Date	Herewith
First Named Inventor	Ryu OGIWARA et al.
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	001701.00198

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
		5,903,492	B1	Takashima	05/1999	
		6,094,370	B1	Takashima	07/2000	
		6,300,654	B1	Corvasce et al.	10/2001	
		6,483,737	B2	Takeuchi et al.	11/2002	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ₆
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
		EP	0 631 287	A	Ramtron Int.	12/1994		X
		DE	197 24 449	A	Toshiba	12/1997		Abst
		JP	10-255483		Toshiba	09/1998		Abst
		JP	11-177036		Toshiba	07/1999		Abst

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		D. Takashima, et al., "Gain Cell Block Architecture for Gigabit-Scale Chain Ferroelectric RAM," 1999 Symposium on VLSI Circuits	
		D. Takashima et al., "High-Density Chain Ferroelectric Random-Access Memory (CFRAM)," Symposium on VLSI Circuits Digest of Technical Papers, 1997, pp. 83-84	
		D. Takashima et al., "A Sub-40ns Random-Access Chain FRAM Architecture with a 7ns Cell-Plate-Line Drive," ISSCC Digest of Technical Papers, February 15, 1999, pp. 102-103, and 450	

Examiner
Signature

Date
Considered

¹EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.